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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/535,984	03/27/2000	Toshiro Obitsu	1614.1045	4143

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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

TRUJILLO, JAMES K

ART UNIT	PAPER NUMBER
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2185

DATE MAILED: 07/17/2003

9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/535,984	OBITSU, TOSHIRO	
	Examiner James K. Trujillo	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 May 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4 and 6-19 is/are rejected.
- 7) Claim(s) 5 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input checked="" type="checkbox"/> Interview Summary (PTO-413) Paper No(s). <u>9</u> . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment A and Extension of Time both dated 5/5/03.
2. Claims 1-19 are presented for examination.

Claim Objections

3. Claims 4 and 5 are objected to because of the following informalities:
 - a. As to claim 4, on line 3 of claim 4, "lease" should be changed to "least".
 - b. As to claim 5, on lines 4-5 of claim 4, "a device unit" should be changed to "the device unit" because further references to "the device unit" are not clear as to which device unit is being referred to (either "a device unit" of claim 5 or "at least one device unit" of claim 4).

Appropriate correction is required.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore,
 - a. the table as per claim 8;
 - b. the judging part as per claims 1, 2, 4, 5, 7-13;

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9Response to Arguments

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
6. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.
7. Claims 1-2, 6, 10, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakashima, U.S. Patent 6,029,211 (referenced in last office action).
8. As to claim 1, Nakashima taught an electronic apparatus comprising:
 - a. a judging part judging whether a combination of a plurality of units is to realize a desired function [a judging part ("selection signal discriminator" of figures 1 and 4, "controller" of figure 2,6, and 7) selects combinations of functions within a PC card are selected to enable a PC card to realize a function, col. 5 lines 16-23, col. 5 lines 41-53, and col. 6 lines 10-19];
 - b. a power supply control part controlling a supply of power from a power source to at least one of said units of said combination used to realize said desired function based on a judgment result of the judging part, based on an aspect of said combination of the

plurality of units [only desired functions are supplied with power ("activated") col. 2 lines 25-28].

Specifically Nakashima teaches a PC card having a plurality of functions. Only the desired functions are powered. Clearly Nakashima must have a power supply to supply only the desired functions and power supply control. Nakashima discloses that a problem with the prior art is that PC cards with multiple function supply power to all functions [col. 1 line 61 through col. 2 line 12]. Here Nakashima discloses that only if a single desired function is activated power must be supplied to the entire card (problem with prior art). Nakashima desirably reduces power consumption to the card by activating only the desired function(s). Therefore activating must be equated to supplying power. Because only selective functions are powered it is inherent that Nakashima must have a power supply control part to effectively control power only to desired functions. Further, Nakashima discloses controlling power by the judging part to a combination of units based upon an aspect of the combination to [col. 6 line 58 through col. 7 line 10].

Please see referenced application 08/984,597 now patent 6,085,982 (Nakashima) for further detailed operation of the invention, which is incorporated by reference by Nakashima.

9. As to claim 2, Nakashima taught the electronic apparatus according to claim 1 described above. Nakashima further teaches wherein the judging part comprises:

- a. an identification information obtaining part [col. 6 lines 43-57] obtaining identification information for identifying from said plurality of units [col. 5 line 58 through col. 6 lines 9]; and

- b. an information judging part judging (selection signal discriminator 12) whether said desired function is realized based on the identification information obtained from said plurality of units [col. 6 lines 13-20].

Specifically, Nakashima has an identification information obtaining part (basic and functional attribute information). This identification information part identifies a plurality of units on each card. The judging part (selection signal discriminator) then selects which functions are to be selected based upon the particular signal.

10. As to claim 6, Nakashima taught the claimed electronic apparatus according to claim 1 described above. Nakashima further teaches wherein the power source is a battery unit [col. 2 lines 1-3].

11. As to claim 10, Nakashima taught a power control apparatus for an electronic apparatus which realizes a desired function by combining a plurality of units comprising:

- a. a judging part judging whether a combination of a plurality of units is to realize the desired function [a judging part (“selection signal discriminator” of figures 1 and 4, “controller” of figure 2,6, and 7) selects combinations of functions within a PC card are selected to enable a PC card to realize a function, col. 5 lines 16-23, col. 5 lines 41-53, and col. 6 lines 10-19];
- b. a power supply control part controlling a supply of power from a power source (must have a power source) to at least one of said units of said combination used to realize said desired function based on a judgment result of the judging part, wherein said judgment is

based on an aspect of said combination of the plurality of units [only desired functions are supplied with power ("activated") col. 2 lines 25-28].

12. As to claims 14 and 15, Nakashima taught the claimed electronic apparatus therefore he taught the method for controlling the power supply.

13. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakashima in view of Jones, U.S. Patent 6,145,046 and Liebenow, U.S. Patent 6,522,640.

14. As to claim 3, Nakashima taught the electronic apparatus according to claim 1 described above. Nakashima did not expressly disclose that the plurality of units are detachable. Nakashima discloses that the units (ATA Memory and a Modem) reside on a PC card. The PC card may be inserted or removed from a slot of a computer removing the plurality of units but not each of the plurality of units separately [col. 5 lines 4-15].

Jones discloses a detachable ATA Memory card [figure 2]. Liebenow discloses a detachable modem [figure 2, col. 4 lines 33-50 and col. 7 lines 1-11].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nakashima by making both his ATA memory and modem detachable as taught by Jones and Liebenow. An artisan would have made the modification because the memory can now be easily changed for a different desired memory size. The detachable modem would allow reduce the cost of the computer while providing wireless communication as described by Liebenow [col. 1 line 53 through col. 2 line 16].

15. Claims 4, 7-9, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakashima.

16. As to claim 4, Nakashima taught the claimed electronic apparatus according to claim 1 described above. Nakashima further taught that information for a specific PC card is available for the computer to read (from the attributes for each function) [figure 3 and corresponding text]. In order for the computer to carry out a function the computer must identify the PC card to be used because an artisan would have recognized that computer systems often use more than one PC card to expand their functionality. In Nakashima a PC card is selected to carry out a function such as operating an ATA memory or a modem. In order to operate the correct device the appropriate device must be identified.

Nakashima also does not expressly disclose the power supply control part stopping the supply of power to the card when the judging part judges that the device unit does not use the PC card (emphasis added). In summary, Nakashima taught a power supply control part activating only the desired function selectively to reduce power consumption, suggesting that power is stopped to unused functioning blocks [col. 2 lines 25-28]. Nakashima discloses that a problem with the prior art is that power is applied to an entire card regardless of the number of functions actually used [col. 2 lines 4-12]. Nakashima solves this by supplying power to only necessary functions. Nakashima does not expressly disclose that if no function were used on the particular card power would be stopped to the entire card.

Official Notice is taken of the motive and modification necessary to implement the ATA memory and Modem on a PC card. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nakashima by implementing the ATA memory and the modem on separate PC cards. An artisan would have been motivated to make the modification because it would allow the ATA memory and modem to be further upgraded as desired.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nakashima by modifying the power supply control part by stopping power to a card when no functions of the card are used. An artisan would have readily recognized the natural extension because Nakashima teaches to supply power to only the necessary functional units. If no functional units were used for a card no functions are needed, therefore all the power to the card should be stopped.

Please see referenced application 08/984,597 now patent 6,085,982 (Nakashima) for further detailed operation incorporated by Nakashima.

17. As to claim 7, Nakashima taught an electronic apparatus connectable to a plurality of units comprising:

- a. a judging part judging whether a combination of a of at least two of said plurality unis [a judging part (“selection signal discriminator” of figures 1 and 4, “controller” of figure 2,6, and 7) selects combinations of functions within a PC card are selected to enable a PC card to realize a function, col. 5 lines 16-23, col. 5 lines 41-53, and col. 6 lines 10-19];
- b. a power supply control part stopping a supply of power to at least one unit in the combination when said judging part judges [only desired functions are supplied with power (“activated”) col. 2 lines 25-28].

In summary, Nakashima teaches an electronic apparatus having multiple functions, wherein multiple functions are used together.

Nakashima does not expressly disclose that the combination of the plurality of units is predetermined. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nakashima by using a predetermined combination of the plurality of units. An artisan would have been motivated to make such a modification because certain units require other a combination of units to execute a function. Having a predetermined function would reduce setup time for the function to be executed such as having a default mode.

18. As to claim 8, Nakashima as modified taught the claimed electronic apparatus according to claim 7 described above. Nakashima does not expressly disclose wherein the judging part comprises a table for storing predetermined combinations of two of said plurality of units, and said judging part judges whether the combination is one of the predetermined combinations based on the table.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Nakashima by using a table to store the predetermined combinations of two of the plurality of units. A table is a well-known data structure that is easy to implement for storing data such as data for Nakashima.

It would have been obvious to one of ordinary skill in the art at the time to use the judging part to judge whether the combination is one of the predetermined combination based on the table because if the combination were a predetermined the system would be able to readily execute the combination. Because the combination is in a table the system would be able to recognize that the combination would work together without further change to the system (i.e. it is a proper combination).

19. As to claim 9, Nakashima as modified taught the claimed electronic apparatus according to claim 7 described above. Nakashima as modified taught a judging part judges whether or not a combination of the plurality of units is the predetermined combination or when said plurality of units are connected to the electronic apparatus as set forth above in the rejection of claim 7.

Nakashima does not expressly disclose wherein the judging part judges whether or not a combination of said plurality of units is the predetermined combination when the electronic apparatus is turned on.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nakashima by using a predetermined combination of the plurality of units. An artisan would have been motivated to make such a modification because certain units require other a combination of units to execute a function. Having a predetermined function would reduce setup time for the function to be executed such as having a default mode.

20. As to claim 11, claim 11 is rejected on the same basis as set forth above in the rejection of claim 7.

21. As to claim 12, claim 12 is rejected on the same basis as set forth hereinabove in the rejection of claim 8.

22. As to claim 13, Nakashima as modified above taught the claimed electronic apparatus, therefore he taught the claimed power control apparatus.

23. As to claim 16, Nakashima as modified above taught the claimed electronic apparatus, therefore he taught the claimed method to operate the apparatus.

24. As to claim 17, Nakashima as modified above taught the claimed electronic apparatus, therefore he taught the claimed method to operate the apparatus.

25. As to claim 18, Nakashima as modified above taught the claimed electronic apparatus therefore he also taught the claimed method of controlling the power supply.

26. As to claim 19, Nakashima as modified above taught the claimed electronic apparatus therefore he also taught the claimed method of controlling the power supply.

Allowable Subject Matter

27. Claim 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,085,982 to Nakashima. This patent teaches removing power from a function on a PC card that is not used.

U.S. Pat. No. 6,381,662 to Harari. This patent teaches a mother card have a detachable daughter card.

U.S. Pat. Appl. Pub. No. US 2002/00131162 to Whitney. This publication teaches a detachable modem that plugs into a PC card.

Japan Pat. No. JP 10075320A to Deguchi. This patent teaches a detachable modem using a PC Card.

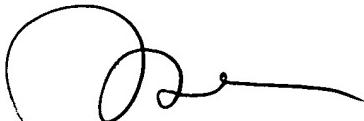
Moghe, S.; Stone, J.; Stratmoen, S.; Consolazio, S.; Rausch, K.; Geske, S.; Patel, M.; "Mobitex PC card wireless modem", Microwave Symposium Digest, 1997, IEEE MTT-S International, Volume: 3, 8-13 June 1997, Page(s): 1391 -1394 vol.3. This paper teaches a PC card wireless modem.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
July 11, 2003



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100